REMARKS

Applicants note that the current Office Action indicates that claim 19 is withdrawn from consideration as being directed to a non-elected invention.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Corisis (United States Patent Number 6,607,937) and Chang (United States Patent Application Publication Number 2002/0153599). Claims 2, 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Corisis, Chang, and Saeki (United States Patent Application Publication Number 2003/0122237). Claim 3 is not explicitly rejected in the Office Action. However, claim 3 is referred to in the Office Action at page 7 as being taught by Corisis. Therefore, the following remarks are based on the belief that the Examiner intended to reject claim 3 under 35 U.S.C. 103(a) based on the combination of Corisis, Chang, and Saeki. In view of the amendments to the claims and the following remarks, it is believed that claims 1-5 and 7 are allowable over the cited references. Accordingly, entry of the amendments and reconsideration of the rejections of claims 1-5 and 7 are respectfully requested.

Independent claim 1 is amended herein to clarify that a multi-chip package comprises a first semiconductor chip, at least one second semiconductor chip, a first connecting unit attached to a surface opposite the back surface of the first semiconductor chip for electrically connecting the first semiconductor chip to an external system, a second connecting unit attached to a surface opposite the back surface of the second semiconductor chip for electrically connecting the second semiconductor chip to the external system, and a printed circuit board for the multi-chip package, which includes bonding pads to which the first connecting unit and the second connecting unit are connected, and pins for connecting the bonding pads to the external system. In addition, claim 1 is amended herein to clarify that the first connecting unit is compatible with, and conductively coupled to, a packaged flash memory of the first semiconductor chip, and the second connecting unit is compatible with the second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to the printed circuit board.

With regard to the rejection of independent claim 1 based on the combination of Corisis and Chang, it is submitted that Corisis and Chang, alone or in combination, fail to

teach or suggest a multi-chip package comprising a first semiconductor chip that includes a packaged flash memory, a first connecting unit that is compatible with, and conductively coupled to, the packaged flash memory, and a second connecting unit that is compatible with a second semiconductor chip in a wafer level configuration and that connects the second semiconductor chip to a printed circuit board, as claimed in amended independent claim 1.

Corisis fails to teach or suggest a first semiconductor chip that includes a flash memory, as claimed in claim 1, and as noted in the Office Action at page 5. Thus, it follows that Corisis does not teach or suggest a first semiconductor chip that includes a packaged flash memory, as claimed in claim 1. Further, it follows that Corisis fails to teach or suggest a first connecting unit that is compatible with, and conductively coupled to, the packaged flash memory of a first semiconductor chip, as claimed in amended independent claim 1. Instead, Corisis teaches a lower packaged device 220a of a microelectronic device assembly 210 that comprises a first microelectronic die 224a (see Corisis, Figure 3). There is no teaching or suggestion in Corisis of the lower packaged device 220a including a packaged flash memory, as claimed in claim 1.

Chang likewise fails to teach or suggest a first semiconductor chip that includes a packaged flash memory, as claimed in claim 1. Instead, as described in Amendment C filed on July 5, 2007, Chang teaches a bottom chip 21 (referred to in the Office Action as a first semiconductor chip) that is an unpackaged flash memory, not a packaged flash memory. This is evident in Chang by bonding wires 26, which are connected to bonding pads of the bottom chip 21 (see Chang, Figure 3 and page 2, paragraph [0009], lines 12-14).

Thus, even if the flash memory of Chang was combined with the microelectronic device assembly 210 of Corisis, there is nevertheless no teaching or suggestion in the combination of Corisis and Chang of a first semiconductor chip including a packaged flash memory, since the lower packaged device 220a of Corisis would include the unpackaged flash memory of Chang, rather than the first microelectronic die 224a of Corisis. However, as described above, neither the microelectronic die 224a of Corisis nor the unpackaged flash memory of Chang is a packaged flash memory, as claimed in claim 1.

In addition, there is no teaching or suggestion in Corisis and Chang, alone or in combination, of a multi-chip package comprising a first connecting unit that is compatible with, and conductively coupled to, a packaged flash memory of a first semiconductor chip, and a second connecting unit that is compatible with a second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to a printed circuit board, as claimed in amended independent claim 1.

Corisis teaches an upper packaged device 220b (referred to in the Office Action at page 3 as a second semiconductor chip) and a lower packaged device 220a (referred to in the Office Action as a first semiconductor chip) (see Corisis, Figure 3). However, since the upper packaged device 220b of Corisis is a packaged device, it follows that the upper packaged device 220b of Corisis is not in a wafer level configuration. Specifically, there is no teaching or suggestion in Corisis of the upper packaged device 220b being a second semiconductor chip in a wafer level configuration, as claimed in amended independent claim 1.

Corisis further teaches a second connecting member 243b that is coupled between the upper packaged device 220b and a bond pad 231b (see Corisis, Figure 3). However, there is no teaching or suggestion in Corisis of the second connecting member 243b being a second connecting unit that is compatible with a second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to a printed circuit board, as claimed in amended independent claim 1.

Chang fails to teach or suggest a first semiconductor chip which shows good results when tested for reliability after being assembled at a package level, as claimed in amended independent claim 1. Specifically, although Chang teaches a multi-chip package 20 comprising an upper chip 22 and a bottom chip 21, there is no teaching or suggestion in Chang of either the upper chip 22 or bottom chip 21 being a first semiconductor chip that is assembled at a package level, as claimed in claim 1.

Further, Chang likewise fails to teach or suggest a second connecting unit that is compatible with a second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to a printed circuit board, as claimed in amended independent claim 1. Instead, Chang teaches second bonding wires 27 that connect the

upper chip 22 to an inner portion 235 of an LOC lead frame (see Chang, Figure 3). There is no teaching or suggestion in Chang of second bonding wires 27 being a second connecting unit that connects the upper chip 22 to a printed circuit board.

Further, Chang likewise fails to teach or suggest a first connecting unit that is compatible with, and conductively coupled to, a packaged flash memory, as claimed in claim 1, since, as described above, there is no teaching or suggestion in Chang of a packaged flash memory. Instead, Chang teaches connectors between pads 25, 24 of the upper and bottom chips 22, 21, respectively, wherein neither upper chip 22 nor bottom chip 21 is assembled at a package level, and wherein neither upper chip 22 nor bottom chip 21 includes a packaged flash memory.

It is therefore submitted that Corisis and Chang, alone or in combination, fail to teach or suggest elements of the invention set forth in claim 1. Specifically, Corisis and Chang each fails to teach or suggest a multi-chip package comprising a first semiconductor chip, at least one second semiconductor chip, a first connecting unit attached to a surface opposite the back surface of the first semiconductor chip for electrically connecting the first semiconductor chip to an external system, a second connecting unit attached to a surface opposite the back surface of the second semiconductor chip for electrically connecting the second semiconductor chip to the external system, and a printed circuit board for the multi-chip package, which includes bonding pads to which the first connecting unit and the second connecting unit are connected, and pins for connecting the bonding pads to the external system. In addition, it is submitted that Corisis and Chang each fails to teach or suggest that the first connecting unit is compatible with, and conductively coupled to, the packaged flash memory, and that the second connecting unit is compatible with the second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to the printed circuit board, as claimed in amended independent claim 1. Accordingly, there is no combination of Corisis and Chang which would provide such teaching or suggestion.

Since the combination of Corisis and Chang fails to teach or suggest the invention set forth in the amended claims, the claims are believed to be allowable over the cited

references. Accordingly, reconsideration of the rejection of claim 1 under 35 U.S.C. 103(a) based on the combination of Corisis and Chang are respectfully requested.

With regard to the rejections of claims 2-5 and 7 under 35 U.S.C. 103(a) based on the combination of Corisis, Chang, and Saeki, it is submitted that Saeki likewise fails to teach or suggest a multi-chip package comprising a first semiconductor chip, at least one second semiconductor chip, a first connecting unit attached to a surface opposite the back surface of the first semiconductor chip for electrically connecting the first semiconductor chip to an external system, a second connecting unit attached to a surface opposite the back surface of the second semiconductor chip for electrically connecting the second semiconductor chip to the external system, and a printed circuit board for the multi-chip package, which includes bonding pads to which the first connecting unit and the second connecting unit are connected, and pins for connecting the bonding pads to the external system, or that the first connecting unit is compatible with, and conductively coupled to, the packaged flash memory, and that the second connecting unit is compatible with the second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to the printed circuit board, as claimed in amended independent claim 1. Instead, Saeki teaches a semiconductor device having a first chip 10A that is a Wafer-level Chip Size Package, which has the function of a package per se (see Saeki, page 2, paragraph [0022]). However, although the first chip 10A has the function of a package per se, there is no teaching or suggestion in Saeki of the first chip 10A comprising a packaged flash memory, as claimed in claim 1. Further, there is no teaching or suggestion in Saeki of a first connecting unit that is compatible with, and conductively coupled to, the packaged flash memory, and a second connecting unit that is compatible with a second semiconductor chip in a wafer level configuration and connects the second semiconductor chip to a printed circuit board, as claimed in amended independent claim 1.

Accordingly, there is no combination of Corisis, Chang, and Saeki which would provide such teaching or suggestion.

Since the combination of Corisis, Chang, and Saeki fails to teach or suggest the invention set forth in the amended claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration of the rejections of claims 2-5 and 7

under 35 U.S.C. 103(a) based on the combination of Corisis, Chang, and Saeki are respectfully requested.

In view of the amendments to and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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